EXHIBIT 1

TO

RESPONDING DECLARATION OF VIVEK SUBRAMANIAN, PH.D.

CLAIMS

1. A metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate having a first concentration of first type impurities;

a drift semiconductor layer formed on a front side of the semiconductor substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region, the JFET region having a third concentration of first type impurities that is greater than the second concentration of first type impurities.

2. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the substrate is a silicon-carbide substrate.

3. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the JFET region has a width of less than about three micrometers.

4. The metal-oxide semiconductor field-effect transistor of claim 3, wherein the JFET region has a width of about one micrometer.

5. The metal-oxide semiconductor field-effect transistor of claim 1, wherein the third concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

6. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a current spreading semiconductor layer formed on a front side of the drift semiconductor layer, wherein the JFET region is formed on a front side of the current spreading semiconductor layer.

7. The metal-oxide semiconductor field-effect transistor of claim 6, wherein the current spreading semiconductor layer has a fourth concentration of first type impurities that is greater than the second concentration of first type impurities.

8. The metal-oxide semiconductor field-effect transistor of claim 7, wherein the fourth concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

9. The metal-oxide semiconductor field-effect transistor of claim 6, wherein the JFET region has a width of about one micrometer.

10. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

11. The metal-oxide semiconductor field-effect transistor of claim 1, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

12. A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

13. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a width of about one micrometer.

14. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

15. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

16. The double-implanted metal-oxide semiconductor field-effect transistor of claim 12, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

17. A double-implanted metal-oxide semiconductor field-effect transistor comprising:

a semiconductor substrate;

a drift semiconductor layer formed on a front side of the semiconductor substrate;

a current spreading semiconductor layer formed on a front side of the drift semiconductor layer;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region, the JFET region being formed on a front side of the current spreading semiconductor layer.

18. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the current spreading semiconductor layer has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities.

19. The double-implanted metal-oxide semiconductor field-effect transistor of claim 18, wherein the first concentration of first type impurities is at least one order of magnitude greater than the second concentration of first type impurities.

20. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, wherein the JFET region has a width of about three micrometers or less.

21. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, further comprising a plurality of base contact regions formed in each of the first and the second source regions, the base contact regions being smaller than the first and second source regions.

22. The double-implanted metal-oxide semiconductor field-effect transistor of claim 17, further comprising a plurality of source regions and a plurality of base contact regions, wherein the plurality of source regions and the plurality of base contact regions form alternating strips of N-type doped regions and P-type doped regions, the alternating strips being substantially orthogonal to respective source electrodes formed over the first and the second source regions.

23. A vertical double-implanted metal-oxide semiconductor field-effect transistor comprising:

a silicon-carbide substrate having a first concentration of first type impurities;

a drift semiconductor layer epitaxially formed on a front side of the silicon-carbide substrate and having a second concentration of first type impurities less than the first concentration of first type impurities;

a current spreading semiconductor layer epitaxially formed on a front side of the drift layer, the current spreading semiconductor layer having a third concentration of first type impurities greater than the second concentration of first type impurities;

a first source region;

a second source region; and

a JFET region defined between the first source region and the second source region and formed on a front side of the current spreading semiconductor layer, the JFET region having a width less than about three micrometers and a fourth concentration of first type impurities greater than the second concentration of first type impurities.